SG SEMICONDUCTOR

RF GaN

NSTIC GaN

National Semiconductor Translation and Innovation Centre (GaN) Technical Capabilities

GaN-on-SiC	**Process**	• Wafer size: 150 mm • Microstrip: 100 µm thickness with backside metallisation and substrate via • Transistor: 0.25 µm gate with source field plate • Interconnection: 2 metal layers
	Demonstrated Devices	**HEMT** • Operating drain voltage: 28 V • Max drain current: 0.9 A/mm • Peak transconductance: 0.38 S/mm • Power density @ 10 GHz: 5 W/mm • Associated power-added efficiency: 45% • Linear gain: 18 dB **MIM** • Capacitance density: 240 pF/mm^2 **Thin-Film Resistor** • Sheet resistance: 50 Ω/□
GaN-on-Si	**Process**	• Wafer size: 200 mm • Microstrip: 100 µm thickness with backside metallisation and substrate via • Transistor: 0.25 µm gate with source field plate • Interconnection: 2 metal layers
	Demonstrated Devices	**HEMT** • Operating drain voltage: 10 – 28 V • Max drain current: 0.9 A/mm • Peak transconductance: 0.31 S/mm • Power density @ 7 GHz, VDS=20 V: 3 W/mm • Associated power-added efficiency: 43% • Linear gain: 12 dB **MIM** • Capacitance density: 240 pF/mm^2 **Thin-Film Resistor** • Sheet resistance: 50 Ω/□

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