SG SEMICONDUCTOR

# Advanced Packaging

Agency for Science, Technology and Research SINGAPORE

## Agency for Science, Technology and Research (A*STAR) Technical Capabilities

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|---|---|---|
| **2.5D Integration** | **Fabrication Capabilities** | • 300 mm redistribution layer (RDL)-first fan-out wafer level packaging (FOWLP) with and without bridge chip<br>• 300 mm FOWLP-based co-packaged optics (CPO)<br>• 300 mm through-silicon via (TSV) interposer and chip-to-wafer (C2W) micro-bump bonding<br>• 200 mm photonic IC (PIC) interposer and C2W micro-bump bonding<br>• 200 mm silicon carbide (SiC) interposer and C2W micro-bump bonding |
| | **Fan-Out Interposer** | • Min RDL line/space: 1 µm<br>• Max number of RDL layers: 7<br>• Min micro-bump pitch: 20 µm<br>• Min C4-bump pitch: 180 µm<br>• Min through-mold interconnect pitch: 60 µm<br>• Max interposer size: 52 x 44 mm |
| | **Through-Silicon Interposer** | • Min RDL line/space: 0.4 µm<br>• Max number of RDL layers: 5<br>• Min micro-bump pitch: 20 µm<br>• Min C4-bump pitch: 180 µm<br>• Min TSV dimension: 10 x 100 µm<br>• Max interposer size: 32 x 26 mm |
| **3D Integration** | **Fabrication Capabilities** | • 300 mm wafer-to-wafer (W2W) and C2W hybrid bonding<br>• 300 mm C2W micro-bump bonding |
| | **Hybrid Bonding** | • Min TSV dimension: 1 x 15 µm<br>• Min W2W hybrid bonding pitch: 0.4 µm<br>• Min C2W hybrid bonding pitch: 2.5 µm<br>• Max W2W hybrid bonding stack: 5<br>• Max C2W hybrid bonding stack: 4 |
| | **Micro-Bump Bonding** | • Min TSV dimension: 5 x 50 µm<br>• Min C2W micro-bump bonding pitch: 20 µm<br>• Max C2W micro-bump stack: 16 |
| **High Heat Flux Chip Cooler** | | • 5 kW @ 10 L/min flow rate using water |

**Connect with us:** info@sgsemiconductor.sg

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| **Cryogenic** | **Fabrication Capabilities** | • 300 mm cryogenic interposer<br>• Die attach and wire bonding that is compatible with cryogenic temperatures<br>• 300 mm surface trapped ion device fabrication |
| | **Cryogenic Interposer** | • Superconducting TSV with α-Tantalum (α-Ta) barrier: 10 x 100 µm<br>• Min Aluminium (Al) RDL line/space: 2 µm<br>• Min Niobium (Nb) RDL line/space: 3 µm<br>• Min Indium (In) solder bump pitch: 80 µm<br>• Min Q-factor of α-Ta resonator: $10^6$ |
| | **Surface Trapped Ion Device** | • Integration of waveguides, grating couplers and ring shape ion trap device on TSV interposer |